REMARKS

No amendments, cancellations, or additions have been made to the claims of the presently claimed case. As such, claims 1-4, 7-12, 15, and 17-25 are currently pending in the case. Further examination and reconsideration of the presently claimed application are respectfully requested.

Objections to the Specification

The Specification was objected to for informalities. As noted above, the Specification has been amended to include the suggested change noted in the Office Action. Since the Specification has been amended for clarifications purposes only, the changes do not present new matter. Consequently, the removal of the objection to the Specification is respectfully requested.

Section 103(a) Rejections

Claims 1-4, 7-12, 15, and 17-25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,093,631 to Jaso et al. (heredinafter referred to as "Jaso") in view of U.S. Patent No. 6,143,663 to Koutny, Jr. (hereinafter referred to as "Koutny"). As will be set forth in more detail below, the § 103(a) rejections are respectfully traversed.

Koutny is not available as prior art for the current rejection. As noted above, claims 1-4, 7-12, 15, and 17-25 were rejected over a combination of Koutny and Jaso. Because the current application has a priority date of August 31, 1998, Koutny is available as prior art against the present claims only under 35 U.S.C. § 102(e). Under the American Inventors Protection Act of 1999 ("the AIPA"), prior art available only under 35 U.S.C. § 102(e) is not usable in a 35 U.S.C. § 103 rejection if the art meets the common ownership requirements of 35 U.S.C. § 103(c) as amended.

The following is a quotation of the revised 35 U.S.C. §103(c) (as of December 14, 2000):

> Subject matter developed by another person, which qualifies as prior art only under one of more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

The AIPA, therefore, amended 35 U.S.C. § 103(c) to state that art which qualifies as prior art only under 35 U.S.C. § 102(e), (f), or (g) is not available for rejections under 35 U.S.C. § 103 if that art was commonly owned or subject to an obligation of assignment at the time the subject invention was made. This change to 35 U.S.C. § 103(c) is effective for any application filed on or after November 29, 1999.

It is noted that upon filing of the present application, the patent to Koutny and the present application were commonly owned by or subject to an obligation of assignment to the same assignee, Cypress Semiconductor Corporation of San Jose, CA. In addition, the present application is an application for patent filed after November 29, 1999 and, thus, is subject to the amendments to § 103(c) made by the AIPA. Consequently, Koutny is not available as prior art against claims of the present application.

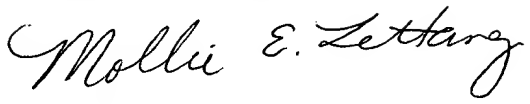
Since Koutny is not available as prior art under the current rejection, no combination of Koutny with other cited art may used for the current rejection. As such, the combination of the references cited in the Office Action for the § 103(a) rejections cannot be used against the presently claimed case. Accordingly, removal of the 35 U.S.C. § 103(a) rejection of claims 1-4, 7-12, 15 and 17-25 is respectfully requested.

CONCLUSION

This response constitutes a complete response to all of the issues raised in the Office Action mailed May 8, 2003. In view of the remarks traversing the rejections, Applicants assert that pending claims 1-4, 7-12, 15, and 17-25 are in condition for allowance. If the Examiner has any questions, comments, or suggestions, the undersigned earnestly requests a telephone conference.

No fees are required for filing this amendment; however, the Commissioner is authorized to charge any additional fees, which may be required or credit any overpayment to Conley Rose, P.C. Deposit Account No. 03-2769/5298-02502.

Respectfully submitted,



Mollie E. Lettang
Reg. No. 48,405
Agent for Applicants

Conley Rose, P.C.
P.O. Box 684908
Austin, TX 78768-4908
Ph: (512) 476-1400
Date: August 6, 2003
MEL

ATTACHMENT A
"Marked-Up" Amendments

IN THE CLAIMS

Please cancel claims 5, 6, 13, 14, and 16. Please amend claims 1, 7, 9, 11, 15, and 17 as follows. Also following is list of all remaining pending claims.

1. (Thrice Amended) A method, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches;

filling said trenches with a conductive material; and

polishing said conductive material to form dummy conductors in said dummy trenches and interconnect in said series of relatively narrow trenches and said relatively wide trench, wherein said [dummy conductors are electrically separate from electrically conductive features of an ensuing integrated circuit] polishing comprises applying a liquid substantially free of particulate matter between an abrasive polishing surface and the conductive material.

2. The method of claim 1, wherein said conductive material comprises a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

3. The method of claim 1, wherein said polishing said conductive material is performed at a substantially uniform polish rate above said dummy trenches and said series of relatively narrow trenches and said relatively wide trench.

4. The method of claim 1, wherein said polishing results in dummy dielectric protrusions between adjacent pairs of said dummy trenches, said dummy dielectric protrusions having first upper surfaces substantially coplanar with second upper surfaces of said dummy conductors.

5. (Canceled)

6. (Canceled)

7. (Amended) The method of claim [5] 1, wherein said abrasive polishing surface comprises particles at least partially fixed into a polymer-based matrix, and wherein said particles comprise a material selected from the group consisting of cerium oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium oxide, chromium oxide, and zirconium oxide.

8. The method of claim 1, wherein said polishing comprises placing a CMP slurry onto a polishing pad surface, and contacting said polishing pad surface with an upper surface of said conductive material while rotating said polishing pad surface relative to said upper surface.

9. (Twice Amended) A method, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a trench which is to receive a relatively wide interconnect feature and a series of trenches which are to receive relatively narrow interconnect features;

filling said plurality of dummy trenches with a conductive material; and

polishing said conductive material to form dummy conductors, wherein said [dummy conductors are electrically separate from electrically conductive features of an ensuing integrated circuit] polishing comprises applying a liquid substantially free of particulate matter between an abrasive polishing surface and the conductive material.

10. The method of claim 9, wherein said conductive material comprises a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

11. (Twice Amended) The method of claim 9, wherein said polishing said conductive material is performed at a substantially uniform polish rate above said dummy trenches and said [said] trench and said series of trenches.

12. The method of claim 9, wherein said polishing results in dummy dielectric protrusions between adjacent pairs of said dummy trenches, said dummy dielectric protrusions having first upper surfaces substantially coplanar with second upper surfaces of said dummy conductors.

13. (Canceled)

14. (Canceled)

15. (Amended) The method of claim [13] 9, wherein said abrasive polishing surface comprises particles at least partially fixed into a polymer-based matrix, and wherein said particles comprise a material selected from the group consisting of cerium oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium oxide, chromium oxide, and zirconium oxide.

16. (Canceled)

17. (Thrice Amended) A substantially planar semiconductor topography, comprising:

a plurality of laterally spaced dummy trenches in a dielectric layer, between a relatively wide trench and a series of relatively narrow trenches, wherein a lateral dimension of at least one of the dummy trenches is less than a lateral dimension of the wide trench and greater than a lateral dimension of at least one of the series of relatively narrow trenches;

dummy conductors in said dummy trenches and electrically separate from electrically conductive features below said dummy conductors; and

conductive lines in said series of relatively narrow trenches and said relatively wide trench, wherein upper surfaces of said conductive lines are substantially coplanar with dummy conductor upper surfaces.

18. The substantially planar semiconductor topography of claim 17, further comprising dummy dielectric protrusions between adjacent pairs of said laterally spaced dummy trenches, said dummy dielectric protrusions having dummy dielectric upper surfaces substantially coplanar with said dummy conductor upper surfaces.

19. The substantially planar semiconductor topography of claim 17, wherein said dummy conductors comprise a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

20. The substantially planar semiconductor topography of claim 17, wherein said interconnect comprise a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

21. The method of claim 1, wherein said dummy conductors are substantially co-planar with said interconnect.

22. The method of claim 9, wherein said dummy conductors are substantially co-planar with said interconnect.

Please add the following claims:

23. (Added) The substantially planar semiconductor topography of claim 17, wherein lateral dimensions of the dummy trenches are between approximately 1 micron and approximately 5 microns.

24. (Added) The substantially planar semiconductor topography of claim 17, wherein the lateral dimension of the wide trench is greater than approximately 50 microns.

25. (Added) The substantially planar semiconductor topography of claim 17, wherein the relatively narrow trenches comprise sub-micron lateral dimensions.